

# Microcontroller Design, Lab (448.029)

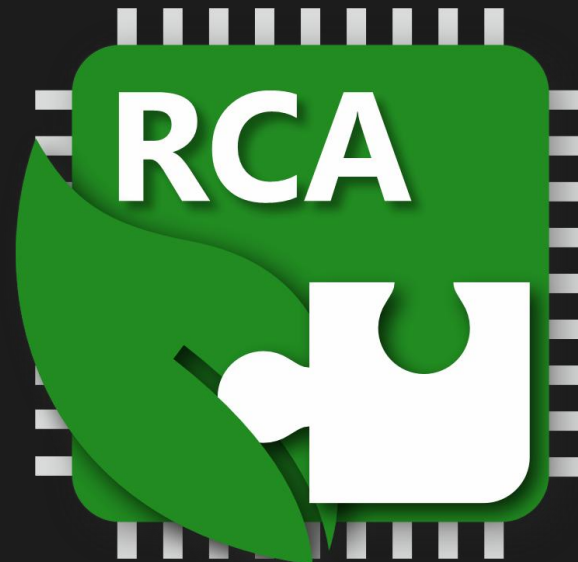
X

 RISC-V<sup>®</sup> Community Challenge with HADES-V

— KICKOFF —

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Reconfigurable Computer Architectures  
Institute of Technical Informatics  
Graz University of Technology



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Tobias Scheipel, TU Graz 2026  
<https://www.scheipel.com>



# Why are we streaming this event?

*This year's iteration of the Microcontroller Design, Lab is featured as official*

**RISC-V<sup>®</sup> International Community Challenge with HADES-V!**

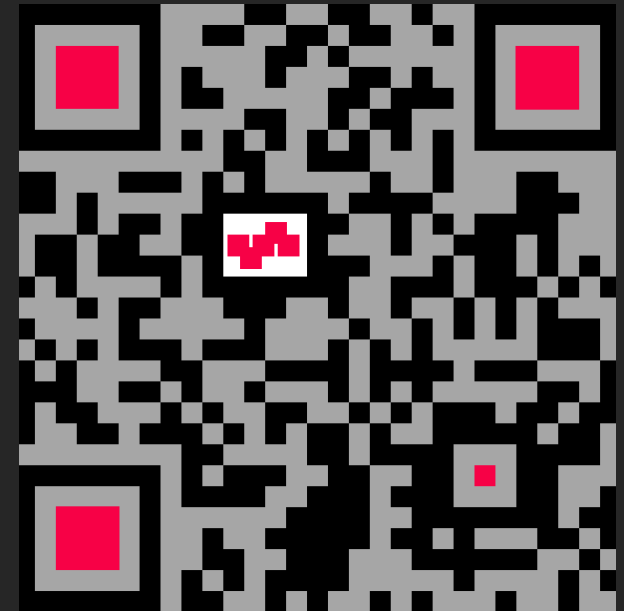


This kickoff event provides information for both the Course and the Community Challenge

## Audience






- **On site:** Graz University of Technology (TU Graz) students attending the course “Microcontroller Design, Lab” (448.029)
- **Online:** Participants of the  **RISC-V**<sup>®</sup> Community Challenge with HADES-V

→ students can also participate in the challenge!  
(and are encouraged to do so!)



# Slide Notation



- >  → general content
- >  → TU Graz course related only
- >  →  RISC-V<sup>®</sup> Community Challenge related only
- >  → technical content



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# Who are we?



## Tobias Scheipel

Assistant Professor  
RISC-V Advocate

## Florian Riedl

PhD student



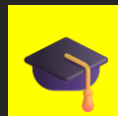
## Michael Neubauer

student tutor

## Simon Schiller

student tutor





# Where are the relevant places @ Inffeldgasse 16?

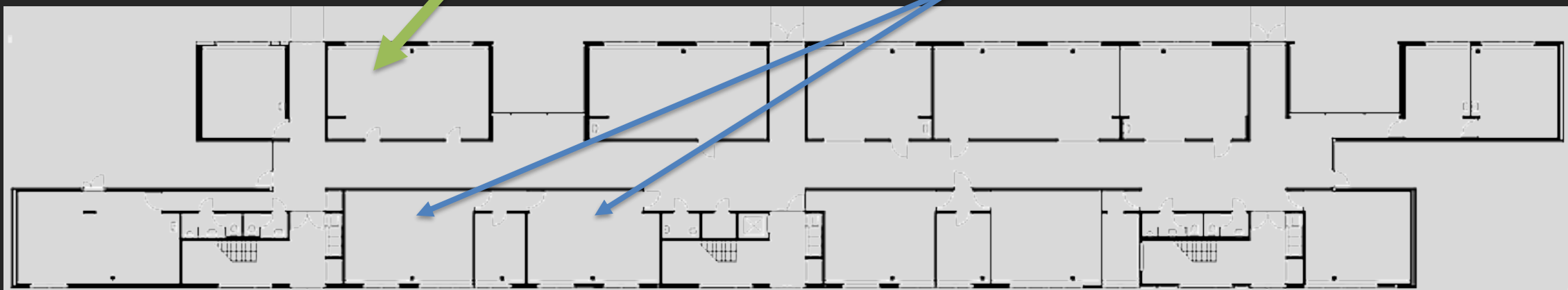


first floor

Tobias Scheipel

Florian Riedl

Lab Rooms  
(EDV3/4, TINO/SO)



ground floor

**consultation by appointment**



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## What is HADES-V ?

- > Open Educational Resource (OER) for microcontroller & processor design
- > build a **pipelined 32-bit RISC-V microcontroller** in SystemVerilog
- > step-by-step, modular “jigsaw puzzle” methodology
  - > implement each stage separately
  - > validate against precompiled golden references
  - > immediate feedback via test system and waveforms

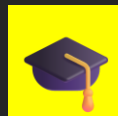




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## After completing, you will be able to

- **design** a complete, modular RISC-V based microcontroller unit using SystemVerilog and standard development environments
- **analyze** the functionality and efficiency of microcontroller designs using verification, synthesis and debugging tools
- **implement** different pipeline stages of a microcontroller using processor architecture knowledge and hardware description languages
- **explain** the execution of software in processors and **evaluate** their interaction with hardware



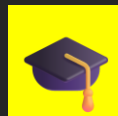
# MDLab Course Organization

## How does a Lab Session work?

- > start at 9 (s.t.!)</li>- > presentation session (attendance compulsory!)
  - > only after submissions: discussion and questions (~1h)
  - > introduction to the next exercise
- > supervised laboratory (attendance voluntary!)
  - > work on exercises (on your own)
  - > time for questions concerning next tasks
  - > supervision by tutors



→ room booked until 1pm



# MDLab Course Organization

## How do I get a grade?

- > 100 total points
- > practical part (75 points)
  - > the tasks build on each other – subsequent errors are included in the evaluation
  - > ΠΕΡΣΕΦΗΟΝΕ grading in action! → [persephone](#) branch of your repo
- > presentation part (25 points)
  - > 2-3 presentations per person; general questions



- > points published in TeachCenter

] 0, 50 ]	] 50, 62 ]	] 62, 75 ]	] 75, 87 ]	] 87, 100 ]
5	4	3	2	1



# How to start?

**join the  
comm  
channels**

**set up  
your  
repository**

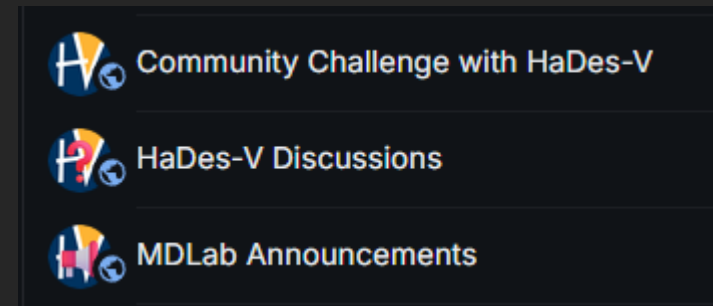
**look into  
the  
Instruction  
Guide**

**download  
the VM  
and  
try stuff**



# Communication Channels

→ join: <https://matrix.to/#/#mdlab:chat.tugraz.at>



- MDLab Announcements → official announcements for course participants @ TU Graz 🎓
- Community Challenge with HADES-V → organizational stuff for the community challenge 🧩
- HADES-V Discussions → technical discussion (self-organized, non-supervised!) 🔧





# Set Up Your Repository

→ fork: <https://github.com/tscheipel/HaDes-V>

## > TU Graz GitLab

### > add "Maintainers":

[tobias.scheipel@tugraz.at](mailto:tobias.scheipel@tugraz.at)

[florian.riedl@tugraz.at](mailto:florian.riedl@tugraz.at)

[michael.neubauer@student.tugraz.at](mailto:michael.neubauer@student.tugraz.at)

[simon.schiller@student.tugraz.at](mailto:simon.schiller@student.tugraz.at)



## > GitHub

### > set Repository to **private**

### > add "collaborators":

[github.com/tscheipel](https://github.com/tscheipel)

[github.com/neubauermichi](https://github.com/neubauermichi)

[github.com/schillersimon](https://github.com/schillersimon)



## > other hosts: set read and write access to [tobias.scheipel@gmail.com](mailto:tobias.scheipel@gmail.com)



## Instruction Guide and other Material

→ look into: <https://doi.org/10.3217/nytm4-grv34>

- Toolchain preparation (already set up in the VM)
- Getting ready (TU Graz GitLab specifics included); includes makefile usage, synthesis description, software upload
- Introduction to the Exercises
- HADESS-V Architecture description (what you actually have to do)





# Introduction to the Exercises → MDLab

→ look into: <https://tc.tugraz.at/main/course/view.php?id=583>

you'll get a grade after first submission, if still registered (a submission is every action you take, e.g., creating a repo, pushing files, your signature)

**deadline for submission:  
sunday before  
presentation day, 23:59pm  
(GIT log)**



#	dates	task	info	pts
1	Mar 03		<i>Introduction</i>	
2	Mar 03		<i>Setup and Kickoff in Lab</i>	
3	Mar 10	1	<b>Presentation:</b> CPU	3
4	Mar 17		<i>Free Lab</i>	
5	Mar 24	2	<b>Presentation:</b> Fetch Stage	8
	Mar 31		holiday	
	Apr 07		holiday	
6	Apr 14	3	<b>Presentation:</b> Decode Stage and Register File	4+4
7	Apr 21		<i>Free Lab</i>	
8	Apr 28	4	<b>Presentation:</b> Decoder	4
9	May 05		<i>Free Lab</i>	
10	May 12	5	<b>Presentation:</b> <i>Execute Stage</i>	10
11	May 19	6	<b>Presentation:</b> Memory Stage	10
	May 26		holiday	
12	Jun 02	7	<b>Presentation:</b> Writeback Stage	16
13	Jun 09		<i>Free Lab (RISC-V Summit Europe!)</i>	
14	Jun 16	8	<i>Free Lab (+ deadline for Synthesize MCU)</i>	6
15	Jun 23	Final	<b>Presentation:</b> Final Exercise	10

# Introduction to the Exercises → Community Challenge



successfully participate in the workshop

mid June

finish the simulation transfer phase



complete exercises 1 – 3

until May 31<sup>st</sup>



## Download the VM and try stuff

→ download: <https://cloud.tugraz.at/index.php/s/xFTeCnZZgca9HsJ>

- › clone your repository (including the code template)
- › open VS code and navigate to the repository
- › execute `make help` and play around with the make commands
- › open `rtl/cpu.sv`, remove the line `ref_cpu golden(.*)`; and get started coding 😊
- › read before you code → the Instruction Guide has a lot of cross references



# Download the VM and try stuff

- › observe the `persephone` branch of your repository

## Testcase Results

Repository: mdlab\_Name\_123456789

Test Run: 03.03.2025 10:00

Test Deadline: 01.01.2025 00:00

## Tested Commit Information

Date: 03.03.2025 09:15

Hash: 4abcd12

Message: Commit message

Committer Email:

## Module Under Test: Fetch Stage

### ▼ Details for the Fetch Stage

Points: 6.94 / 8

### delayed wishbone acknowledge

### ack 1 cycle delayed

Test input: status\_backwards\_in = READY, wb.ack = 1, wb.err = 0

# How do we start into the Lab now?

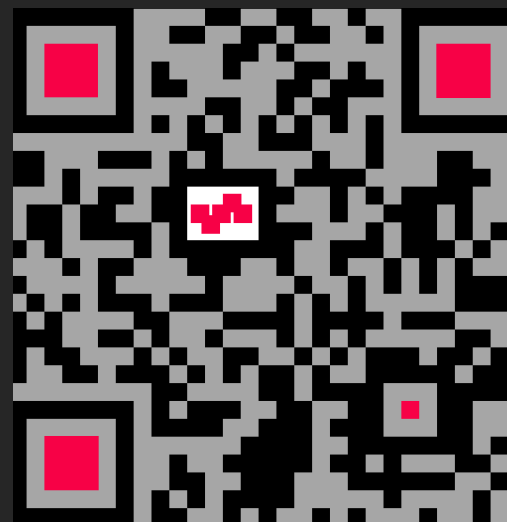
- group registration starts now (9:30)!
- G1/2 downstairs, G3/4 upstairs  
→ distribute evenly!
- follow your tutor to your lab room according to your group
- download the Instruction Guide and start reading 😊





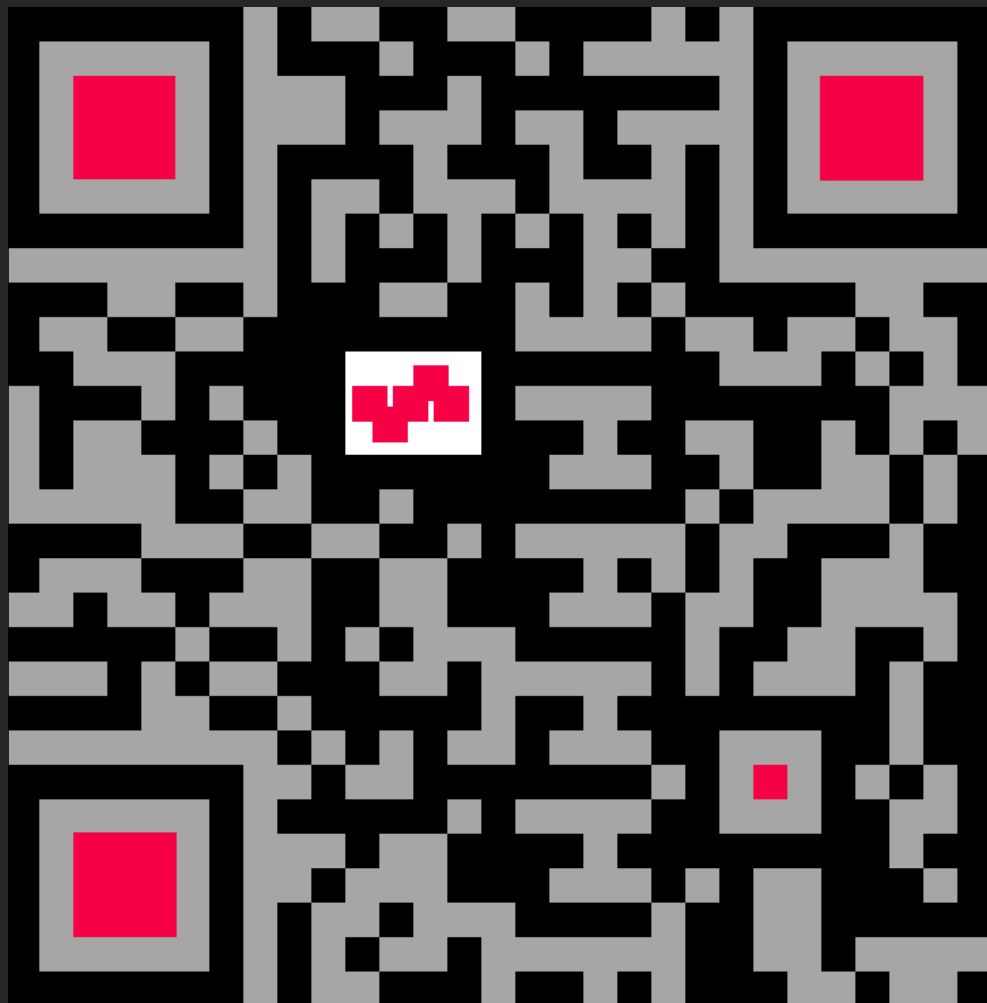
## How do we start into the Challenge now?

- make sure you are officially registered
- create and setup your repo
- download the Instruction Guide and start reading 😊



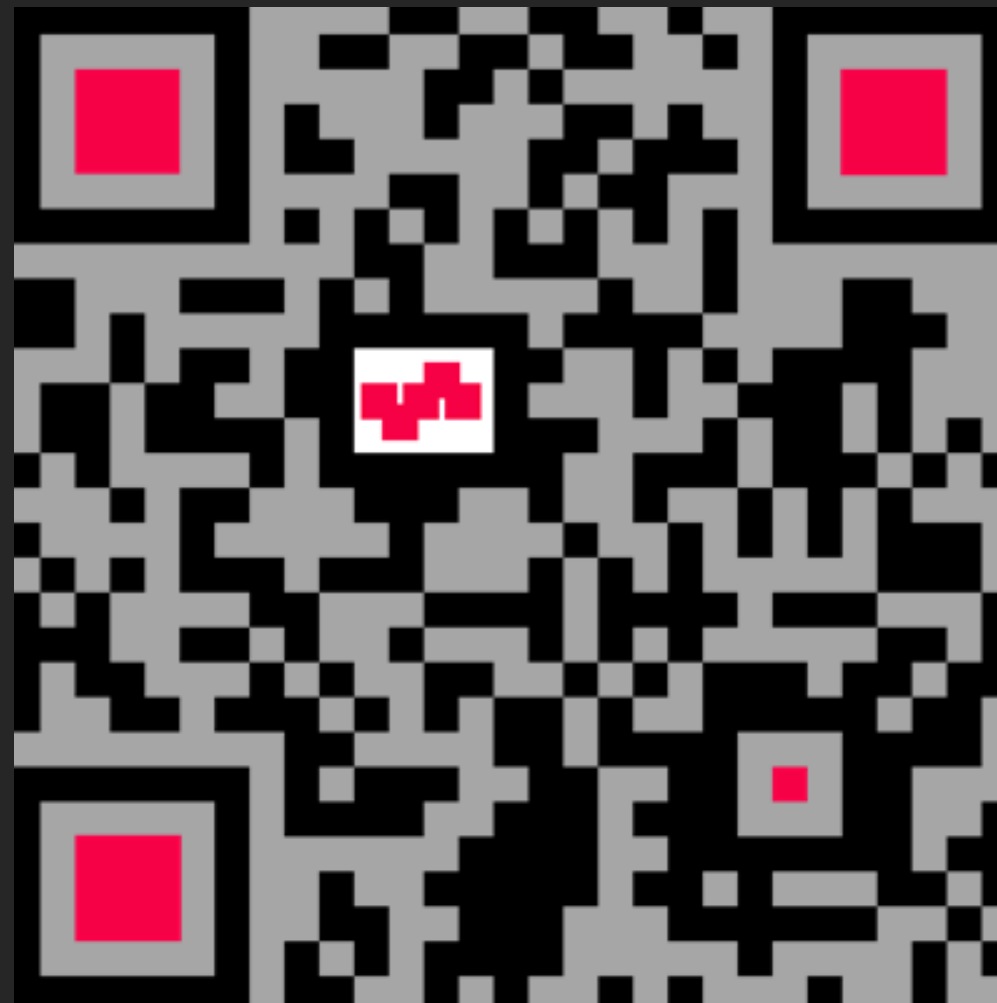


# HADES-V Material Hub



[scheipel.com/hades-v](https://scheipel.com/hades-v)

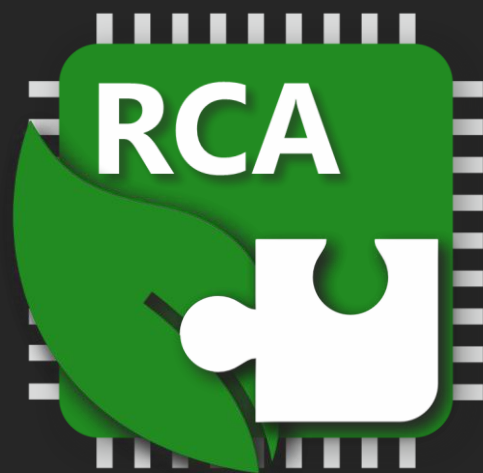
# Community Challenge



[community.riscv.org/e/mp8k48/](https://community.riscv.org/e/mp8k48/)

Thank you for your Attention!

Questions?



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Tobias Scheipel, TU Graz 2026

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