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RISC-V-based Hardware Accelerators

Mustafa Alkhazraji, MSc.

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Overview

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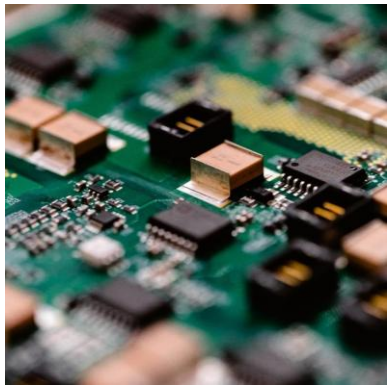
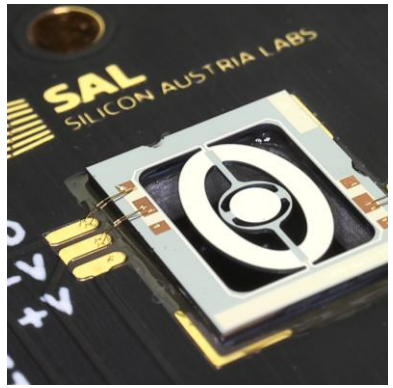
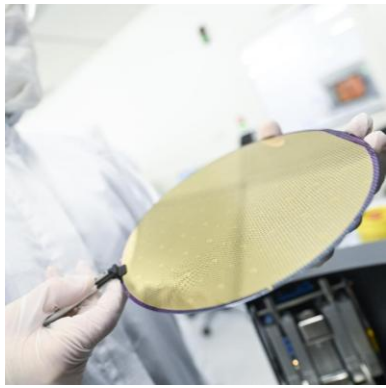
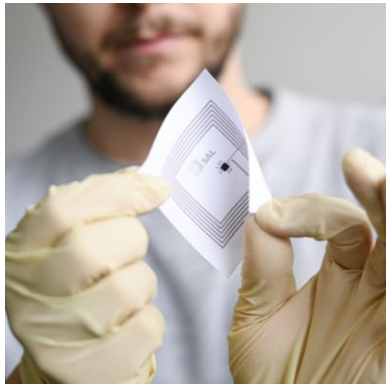
What do we do?

Silicon Austria Labs (SAL), established in 2018, is a European **R&D center** with a focus on the development of efficient and trustworthy technologies in the field of **electronic systems.**

- Industry-oriented research
- Well-equipped research infrastructure
- Customized opportunities for co-operation



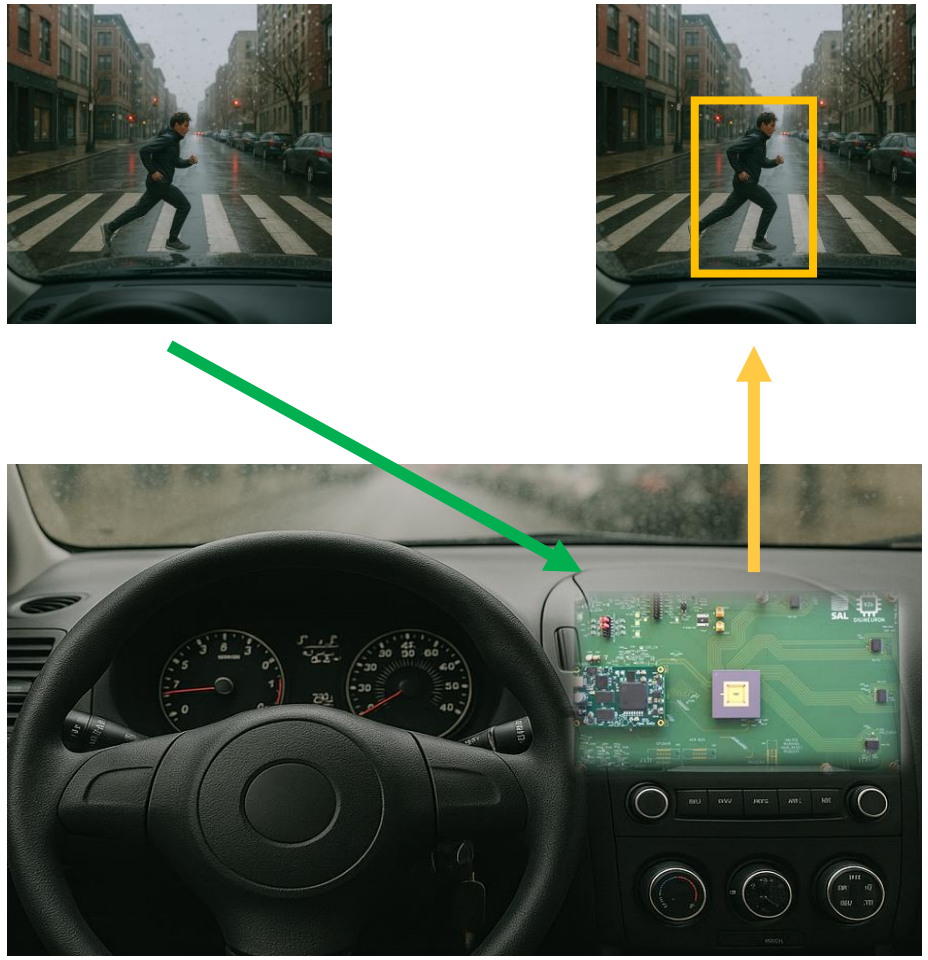
AI ACCELERATION- FOR EVENT CAM.

Research Focus

Edge AI Acceleration: Speed up neural network processing for efficient, low-latency AI on edge devices.

Objectives

- **Efficient Edge Devices:** Reduced latency, power consumption, and privacy risks through local AI acceleration.
- **RISC-V Ecosystem Integration**: RISC-V supports customizable, cost-effective hardware-software co-development for edge and AI-centric applications.

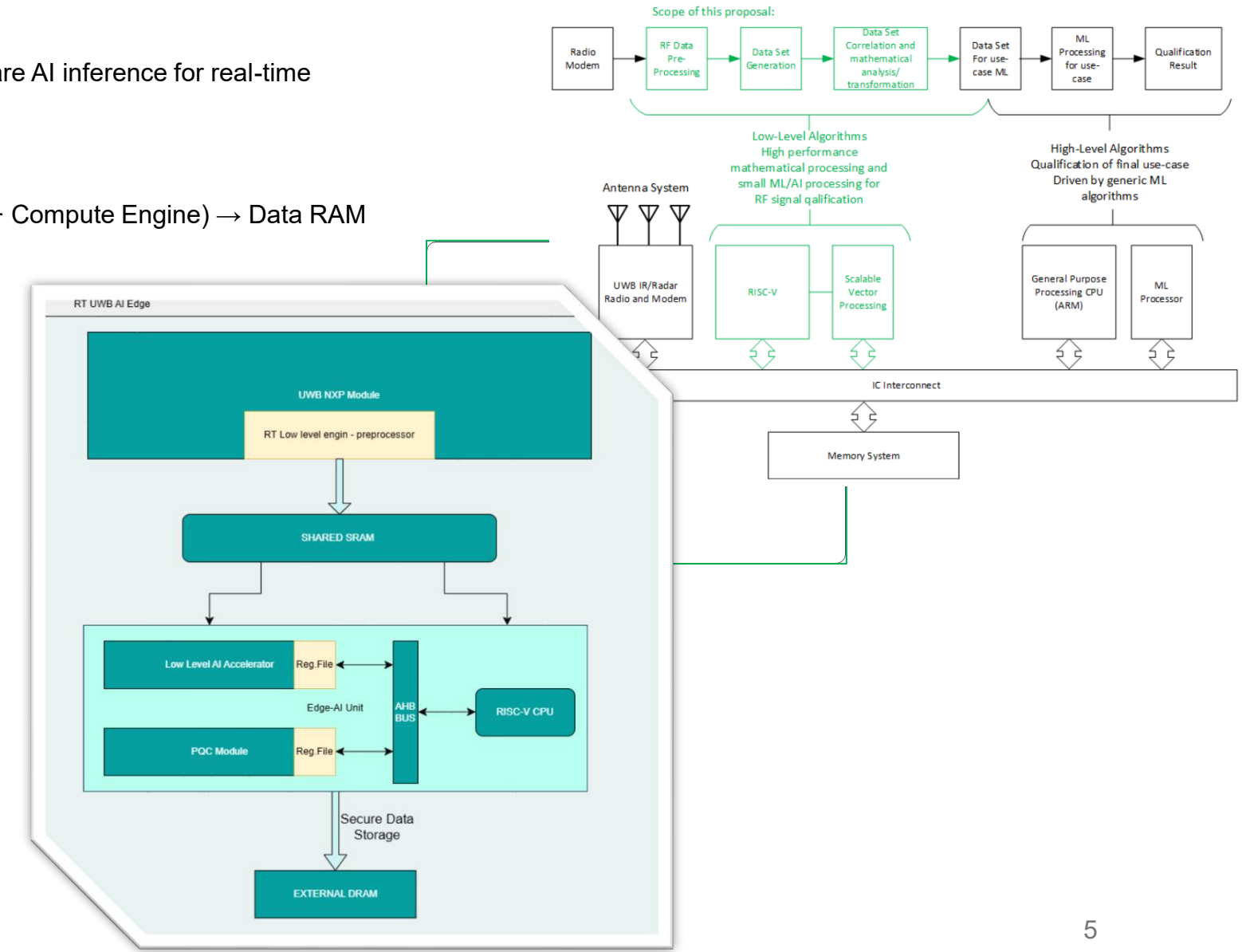


AI ACCELERATION- FOR UWB RADAR.

- Goal:
  - Enhance UWB radar detection by adding hardware AI inference for real-time classification.

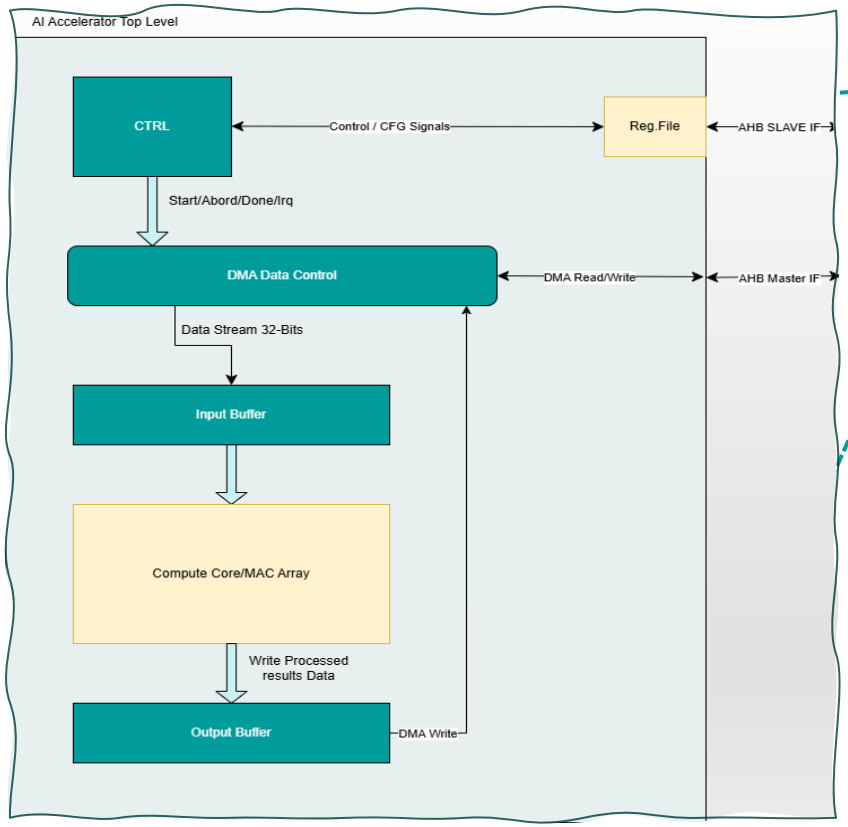
- High-Level Data Flow:
  - UWB → Shared SRAM → AI Accelerator (DMA + Compute Engine) → Data RAM → Host

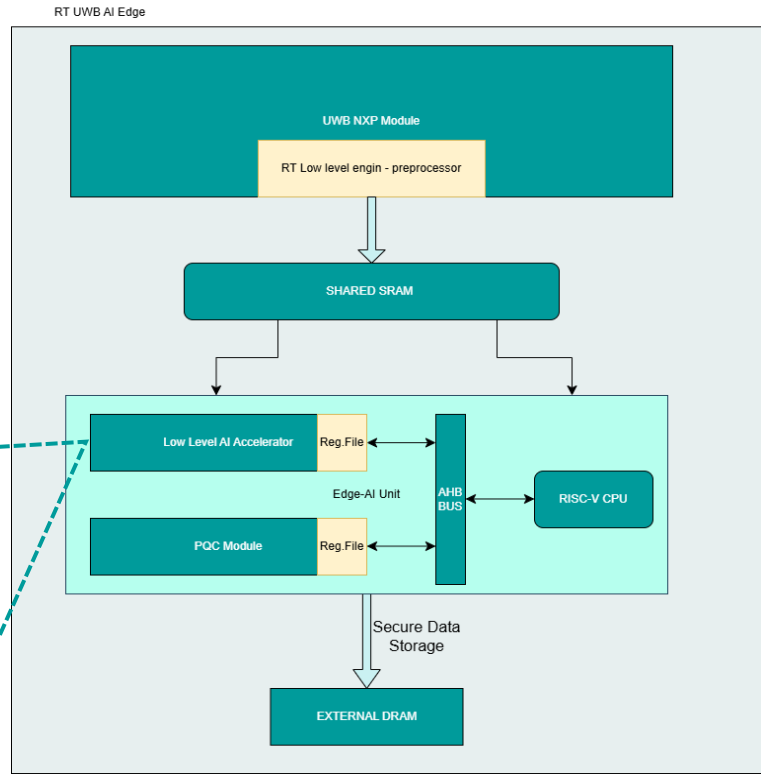
- Why Acceleration?
  - High frame rate (500–1000 Hz)
  - Complex I/Q processing
  - Need <1 ms latency
  - ML-based classification improves reliability vs thresholding



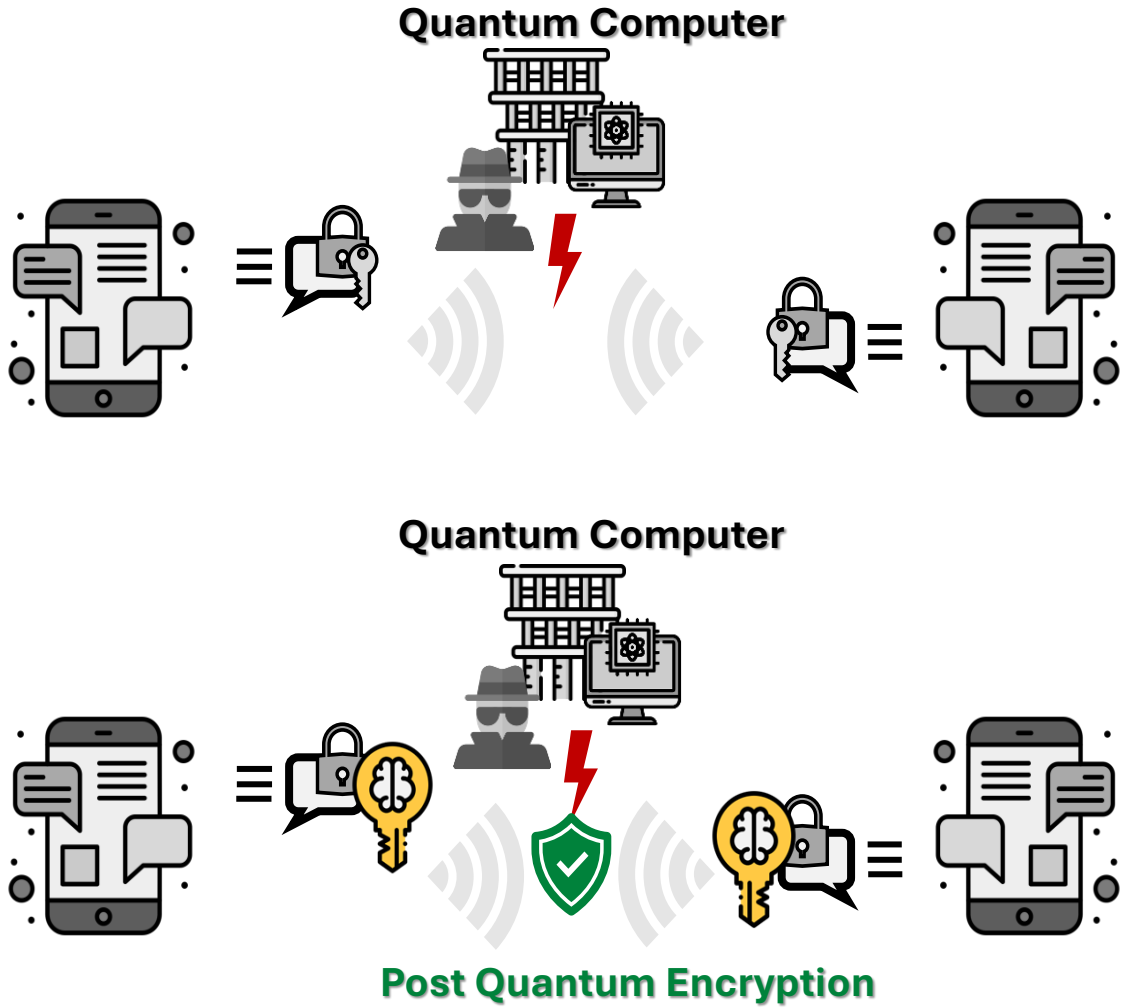
END-TO-END PROCESSING PIPELINE

- UWB Writes CIR → Shared SRAM
- RISC-V Detects New Frame
- DMA Loads CIR Into Input Buffer
- Compute Engine Processes Frame:
  - Feature extraction
  - Magnitude & filtering
  - Dense/FNN inference (future)
- DMA Writes Results → Data RAM
- RISC-V Signals Completion Interrupt





POST-QUANTUM ENCRYPTION



Research Focus

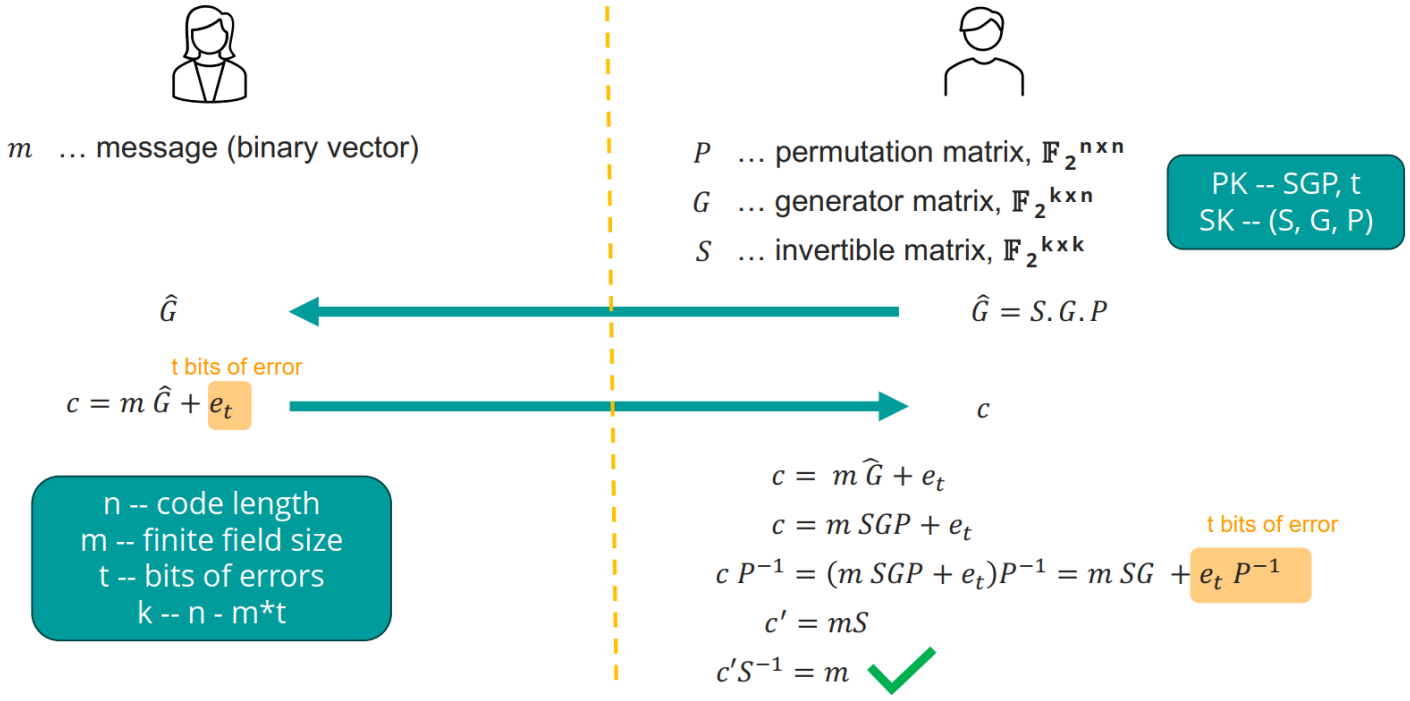
Post Quantum Cryptography (PQC) Acceleration: Optimize post-quantum cryptography algorithms for use in constrained environments.

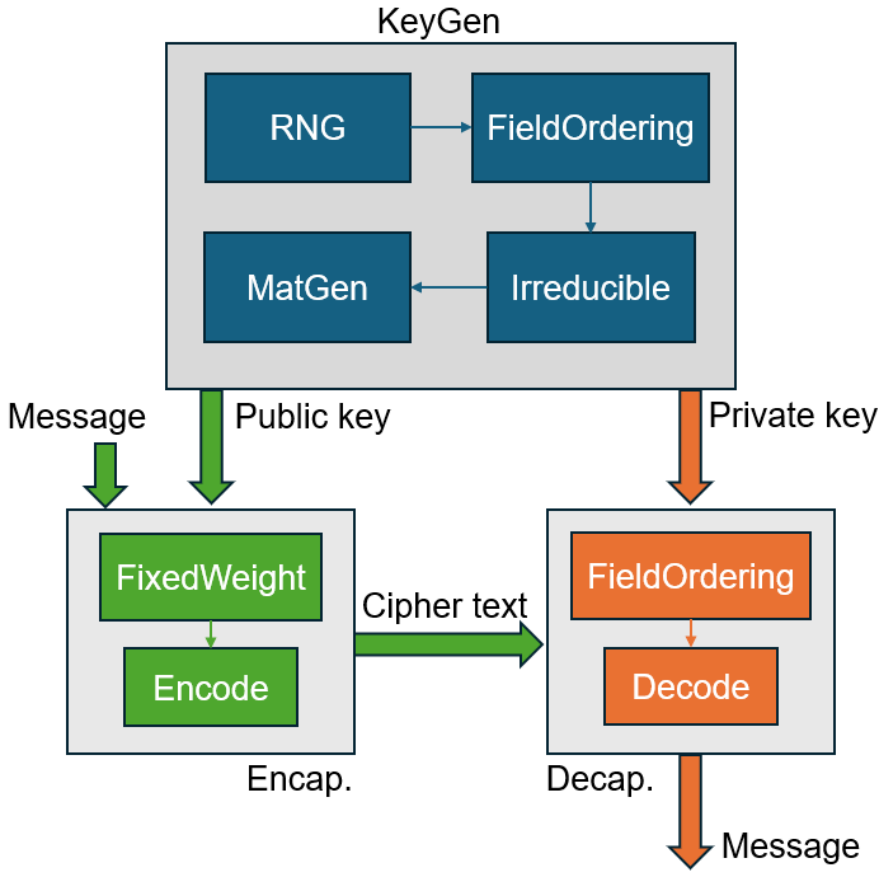
Objectives

- **Efficient Edge Devices:** Reduced latency, power consumption, and privacy risks.
- **Security:** Quantum-safe encryption that keeps up even in the most resource-constrained edge environments.
- **RISC-V Ecosystem Integration**: RISC-V supports customizable, cost-effective hardware-software co-development for edge and AI-centric applications.

THE MCELIECE CRYPTO SYSTEM

- **Fast decryption and encryption, small ciphertext, SCA hardening**
- **Proven resilience** (since 1978) for high-security applications (military, space)
- **Large key sizes** - Handling of large memory



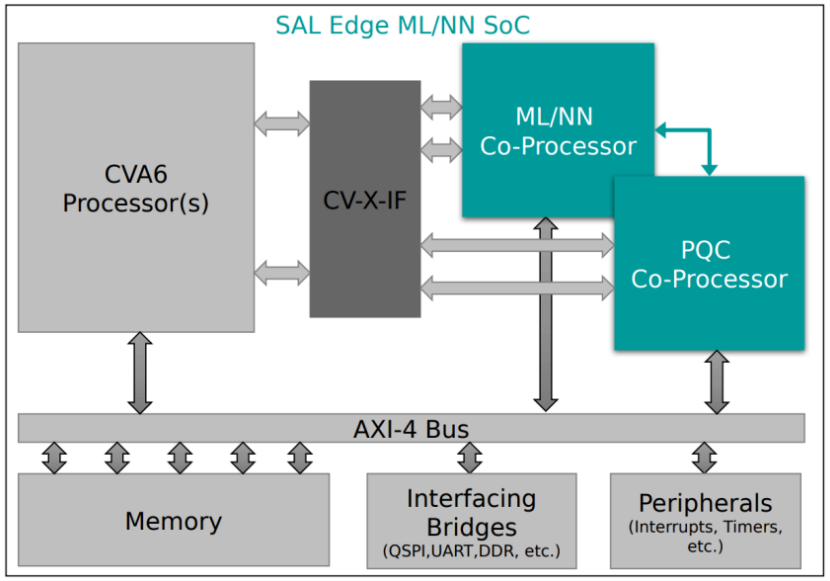


SUMMARY AND FUTURE

- RISC-V + NN accelerators
  - Enables inference operations on the edge – low power + area cost
  - Capabilities for tapeout, bring-up, and lab testing
- The CM cryptosystem
  - Primitives can be reused for multiple applications – PQC or otherwise
  - Current design is WIP – but feasible approach for embedded HW in timing & area estimates
- RISC-V based design – seamless integration of toolchains, simulator, peripheral IPs
  - Tightly coupled coprocessors through X-IF
- Chips-JU projects play a crucial role in advancing the RISC-V ecosystem

Future plans

- SoC for acceleration of distributed learning tasks via Quantum-Safe Cryptography
- Integration of the FW and SW framework (LLVM/MLIR)



CURRENT PROJECTS

- H**I**gh Performance, **S**afe, Secure, **O**pen-Source **L**everaged RISC-V **D**omain-Specific **E**cosystems
- Chips-JU + FFG funding for Austrian partners
- Around 40 partners from 9 countries
- Enhance European high-performance RISC-V-based Systems-on-a-Chip (SoC)
- Development of advanced architectures, novel accelerators, and reusable IPs

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